REMARKS

Claims 2-6 and 8-10 remain in the application for consideration of the Examiner with Claims 1, 7, and 11-14 standing cancelled.

Reconsideration and withdrawal of the outstanding rejection are respectfully requested in light of the above amendments and following remarks.

Turning now to the art rejections, Claims 1 and 2 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yasuda; Claims 1, 2, 7, 8, 11, and 12 were rejected under 35 U.S.C. § 102(e) as being anticipated by Scheurenbrand; Claims 1, 2, 7, 8, 11, and 12 were rejected under 35 U.S.C. § 102(b) as being anticipated by Higuchi; and Claims 3-6, 9, 10, 13, and 14 were rejected under 35 U.S.C. § 103 as being unpatentable over Yasuda, Scheurenbrand, or Higuchi in view of Applicant's discussion.

These rejections are respectively traversed.

It is respectfully submitted that Yasuda does not disclose or suggest the presently claimed invention including the linearization circuit including an analog to digital converter to digitize the position indication signal and a programmed digital signal processor to produce a linear command signal output from the analog position indication signal in independent Claim 3, a analog-to-digital converter for receiving the analog position indicating signals to convert the analog position indicating signal to a digital position indicating signal, a digital signal processor for receiving the digital position indicating signal, the DSP being programmed to convert the digital position indicating signal into a digital signal that is linear proportional to the position of the moveable member and a digital-to-analog converter for receiving the digital signal that is linear proportioned to a position of the moveable member for producing a linear analog positioning signal in independent Claim 4, albeit defined as the linearization, the analog position including digitizing the analog positional position indicating signal and performing the linearization in a program DSP in independent Claim 10.

Scheurenbrand does not disclose or suggest the presently claimed invention including the linearization circuit including analog-to-digital converter to digitize the position indication signal and a program digital signal processor to produce a linear command signal output from the analog position indication signal as defined in the various forms in independent Claims 3, 4, and 10.

It is respectfully submitted that Higuchi does not disclose or suggest the presently claimed invention including the linearization circuit including an analog-to-digital converter to digitize the position indication signal and a programmed digital signal processor to produce a linear command signal output from the analog position indication signal as defined in the various forms in independent Claims 3, 4, and 10.

Applicants agree with the Examiner as evidence by page 6 of the Office Action that none of the above references shows a linearization circuit that includes an analog-to-digital converter to digitalize the position indication signal and a program digital signal processor to produce a linear command signal output from the analog position indication signal, an analog-to-digital converter for receiving the analog position indicating signal to convert the analog position indication signal to a digital position indication signal, a digital signal processor for receiving the digital signal indications signals, the DSP being programmed to convert to digital position indicating signal into a digital signal that is linear proportional to a position of the moveable memory the digital analog converter for converting the digital signal that is linear proportional to the position of the moveable member for producing an linear analog positioning command and a voltage amplifier for receiving the linear analog position command to produce a position voltage and for application to the moveable member.

Applicants additionally agree that none of the above references discloses a DSP to scale the digital position signal in production of the digital signal and linear proportion to the proportion of the moveable memory.

The present invention states that circuit 40 can be readily produced using available circuit and techniques and processes. The Examiner allegedly and erroneously concludes that it would have been obvious of one ordinarily skilled in the art to employ the known circuit cited by Applicant in the device of any of Yasuda, Scheurenbrand, or Huguchi.

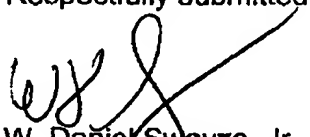
However, Applicants have not admitted that the circuit is known in the art. And consequently reject the Examiner's contention that such a circuit is obvious based on the known teachings.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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